AMMENDMENTS TO THE DRAWINGS

Please replace Figure 5A with the attached Figure 5A Replacement Sheet.

REMARKS

Amendments to the Specification

Paragraphs [0038], [0045], [0046], [0064] and [0066] of the Specification have been amended. These amendments are made to correct typographical errors. Paragraphs [0038] and [0045]-[0046] were amended to address reference number inconsistencies between paragraph [0038] and Figure 2A, paragraph [0045] and Figure 3A and paragraph [0046] and Figure 3B. Paragraph [0064] was amended to correct a reference made to reference number "301" which does not appear in Figure 3. The reference in paragraph [0064] should refer to reference number "310" which appears in Figure 3A. Paragraph [0066] was amended along with Figure 5A to address an issue where reference number 530 is used in reference to two different features in the Figure. Applicant respectfully submits that making the amendments to correct the typographical errors would be obvious to a casual observer and no new matter has been introduced thereby.

Amendments to the Drawings

Figure 5A has been amended to correct a duplicate reference number (530) used in the Figure. A Replacement Sheet is attached to this Office Action Response. Applicant submits that this amendment is supported by the Specification and introduces no new matter thereby. Paragraph [0066] has been appropriately amended to address the amendment to Figure 5A.

Response to Examiner's Comments

Applicant respectfully disagrees with the Examiner's comments in Element 10 of Pages 10-11 of the Final Office Action mailed on January 25, 2007, where the Examiner stated that "[a]pplicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Applicant has provided a definition on page 6 of the Amendment and has asserted that each individual references does not teach the invention as defined in the definition. Definitions in the specification are not read into the claims unless the term is explicitly used in the claim language. Additionally, the Applicant has provided mere allegations that the references do not teach the

claimed invention. The Applicant has to clearly point out why/how the combination of the references fail to teach the claimed invention to overcome the rejection. Additionally, it should be noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In *re Keller,* 642 F.2d 413,208 USPQ 871 (CCPA 1981); In *re Merck & Co.,* 800 F.2d 1091,231 USPQ 375 (Fed. Cir. 1986)."

Applicant respectfully contends that Applicant has, herein and in Applicant's Response mailed on October 25, 2006, rebutted the cited references individually and in combination and thus comply with 37 CFR 1.111(b), contrary to the Examiner's assertion. Applicant also respectfully maintains that Applicant has defined the claims terms "split data" and "non-split data" in the Specification. In addition, Applicant respectfully notes that the Examiner did not comment on or rebut the Applicant's other additional arguments against the rejection of claims 1-6, 29-32, 38-40, 44, 67, 63-64, 68-70, 73-74, 83, 85-88, 93-95, 98 and 101, regarding the references Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. stated on pages 6-8 of the Response mailed on October 25, 2006. Applicant specifically notes that the Examiner did not address Applicant's assertion that neither Estakhri et al, Iwata et al., Harper, III et al., Gonzales et al., or Miura et al. taught or suggested, either alone or in combination, a Flash memory with a modified copy back command or operation or control circuits for managing the same.

Applicant notes that MPEP § 2142 states that a prima facie case of obviousness under 35 U.S.C. § 103(a) is established when three basic criteria are met. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See,* MPEP §2142 and 2141. Thus Applicant respectfully contends that when elements relied upon in the references in making a rejection under 35 U.S.C. § 103(a) are shown to not be disclosed or suggested by the cited references, either alone or in combination, the rejection under 35 U.S.C. § 103(a) cannot be sustained. Specifically, Applicant contends that the elements of split data and modified copy back command were shown by Applicant, both herein and in the Response of

October 25, 2006, to have not been disclosed or suggested by the cited references of Estakhri et al, Iwata et al., Harper, III et al., Gonzales et al., or Miura et al., either alone or in combination.

Applicant understands that the Examiner is required to read the claims broadly. However, as stated by MPEP §2111 and § 2173.01, this reading must be done to give the pending claims their "broadest reasonable interpretation consistent with the specification," and that "[t]he broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." In addition, as stated in MPEP §2111.01, "the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification," and that "[a]n applicant is entitled to be his or her own lexicographer and may rebut the presumption that claim terms are to be given their ordinary and customary meaning by clearly setting forth a definition of the term that is different from its ordinary and customary meaning(s)."

Applicant notes that Applicant's Specification discloses both split data and non-split data embodiments utilizing a modified copy back command. As stated previously, Applicant notes that the Specification of the Present Application defines a split data non-volatile memory devices or systems as having split user/overhead data that avoids the issue of potential corruption of both the user data and overhead data due to each being held within close proximity to each other or on the same physical row (wordline), and super blocks as pairs of erase blocks where when user data is read from a sector of an erase block of the Flash memory 200, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. Applicant contends that the Specification specifically defines what the terms "split data" and "non-split data" mean, in at least Paragraphs [0010], [0025], [0035] and [0038], and also contends that these terms are so utilized in the claims. Applicant also notes that a modified copy-back operation utilizing a sequence of NAND commands that read the source physical pages into internal data latches of the memory device, optionally transfer selected data bytes/sectors from the internal data latches external to the memory device, mask off the data in the latches that is not to be moved, and write the modified latch data to a target physical page. Applicant contends that the Specification specifically defines what the term "modified copy-back" means, in at least Figures 5A and 5B, and Paragraphs [0010], [0043]-[0044], [0049], and [0065]-[0070], and also contends that this term is so utilized in the claims.

In the Response of October 25, 2006 and herein, Applicant specifically notes these definitions of the terms "split data," "non-split data" and "modified copy-back" in the Specification. Applicant also specifically notes that these elements and their underlying circuits and function are not disclosed or suggested by the cited references of Estakhri et al, Iwata et al., Harper, III et al., Gonzales et al., or Miura et al., either alone or in combination, as detailed below and in the Response of October 25, 2006.

Applicant therefore respectfully disagrees with the Examiner's assessment of the limitations of the claims and maintains that the Examiner is impermissibly reading interpretation of the claims that is contrary to the definitions of the terms and limitations of the claims in the Specification. Applicant also respectfully maintains that the cited references of Estakhri et al, Iwata et al., Harper, III et al., Gonzales et al., or Miura et al., have not been shown to disclose or suggest these limitations, either alone or in combination.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6, 29-32, 38-40, 44, 67, 69-70, 73-74, 85-88, 93-95, 98 and 101 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Harper III, et al.(U.S. Patent No. 4,918,600). Claims 7, 33 and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Harper III, et al. (U.S. Patent No. 4,918,600) as applied to claim 1 above and further in view of Miura et al. (U.S. Published Application No. 2006/0041711). Claims 8-9, 11-14, 16-17, 20-21, 25-26, 36, 45, 75-76, 78, 84, 89-92 and 102 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Gonzalez et al. (U.S. Patent No. 7,032,065). Claims 15, 19, 27 and 79 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918) in view of Iwata et al. (U.S. Published Application No. 2004/0193774) and Gonzalez et al. (U.S. Patent No. 7,032,065) as applied to claim 8 above and further in view of Miura et al. (U.S. Published Application No. 2006/0041711). Applicant respectfully traverses these rejections and submits

that claims 1-9, 11-17, 19-21, 25-27, 29-33, 36, 38-41, 44-45, 67, 69-70, 73-76, 78-79, 84-95, 98 and 101-102, as pending, are allowable for at least the following reasons.

As stated above, Applicant respectfully maintains that the Specification of the Present Application defines a split data non-volatile memory devices or systems as having split user/overhead data that avoids the issue of potential corruption of both the user data and overhead data due to each being held within close proximity to each other or on the same physical row (wordline), and super blocks as pairs of erase blocks where when user data is read from a sector of an erase block of the Flash memory 200, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. *See*, Paragraphs [0010], [0025], [0035] and [0038] of the Specification of the Present Application. Applicant also notes that a modified copy-back operation utilizing a sequence of NAND commands that read the source physical pages into internal data latches of the memory device, optionally transfer selected data bytes/sectors from the internal data latches external to the memory device, mask off the data in the latches that is not to be moved, and write the modified latch data to a target physical page. Applicant contends that the Specification specifically defines what the term "modified copy-back" means, in at least Figures 5A and 5B, and Paragraphs [0010], [0043]-[0044], [0049], and [0065]-[0070], and also contends that this term is so utilized in the claims.

In regards to Estakhri et al. – Applicant respectfully maintains that Estakhri et al. discloses a parallel erasing Flash memory system that groups an erase block from each Flash memory device in the system into a "super block" and erases them in parallel, reducing the overall erase time from that of serially erasing the same number of erase blocks from a single Flash memory device. *See, e.g.*, Estakhri et al., Figure 2; Column 2, line 62 to Column 3 Line 54; and Column 9, Line 7 to Column 10, Line 23.

As noted by the Examiner, Applicant therefore submits that Estakhri et al does not teach or suggest a copy-back or a modified copy-back command. Applicant also submits that Estakhri et al. does not teach or suggest a split data non-volatile memory device or system that has split user/overhead data or super blocks wherein the user data and overhead data of a given sector are not stored within close proximity to each other or on the same physical row (wordline) or super

blocks, wherein each super block contains a pair of erase blocks where user data is read from a sector of an erase block of the super block, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. As such, Applicant submits that Estakhri et al. does not teach or suggest each and every element of the Applicant's claimed invention.

In regards to Iwata et al. – Applicant respectfully maintains that Iwata et al. discloses a Flash memory card that has a Flash controller with an erase block data merge circuit which operates to consolidate data to a new erase block from an old erase block and subsequent erasure of the old erase block, which is accomplished by externally reading the data from the old erase block with the Flash controller and writing it to the new erase block. Applicant maintains that, in disclosing an external data merge circuit and operation, Iwata et al. does not disclose split data (storing user data in a differing word line or erase block from the associated overhead data) or a Flash memory with an internal copy-back or an internal modified copy back command or operation or control circuits for managing the same. As noted by the Examiner, Iwata et al. also does not teach masking the read data. *See, e.g.*, Iwata et al., Abstract; Figures 1, 4 and 5; Paragraphs [0016]-[0079] and [0111]-[0142]. Applicant thus submits that Iwata et al. does not teach or suggest a split or a non-split data move circuit or method utilizing an internal modified copy back operation in a non-volatile memory. As such, Applicant submits that Iwata et al does not teach or suggest each and every element of the Applicant's claimed invention.

In regards to Harper, III et al. – Applicant respectfully maintains that Harper, III et al. discloses a memory system for dynamic address mapping for vector access in a memory system and not a non-volatile memory system. . Applicant maintains that Harper, III et al. does not disclose split data (storing user data in a differing word line or erase block from the associated overhead data) or a Flash memory with an internal copy-back or an internal modified copy back command or operation or control circuits for managing the same. Applicant also submits that Harper III, et al. does not disclose masking of data sectors read from the memory or masking of data in a modified copy back operation, but the masking of a row address field. *See, e.g.*, Harper, III et al., Figure 1; Column 14, lines 38-47; Abstract. Applicant thus submits that Harper, III et al. does not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory. As such, Applicant submits

that Harper, III et al. does not teach or suggest each and every element of the Applicant's claimed invention.

The Examiner also maintained that, while Iwata et al. and Harper, III et al. only disclose transferring the entire read data to the target block, it would be obvious to one skilled in the art to write portions of the read data and not the entire amount of data read. Applicant respectfully disagrees and contends that there is no motivation or suggestion to modify the references in the manner suggested by the Examiner. Specifically, Applicant notes that as stated in the Specification at Paragraph [0031], copy-back commands typically do not allow for read out or masking of the data being transferred. In addition, as maintained above, since neither Estakhri et al., Iwata et al. and Harper, III et al. disclose a Flash memory with an internal copy-back or an internal modified copy back command or operation or control circuits for managing the same, to modify Estakhri et al., Iwata et al. and Harper, III et al. to allow for read out or masking of the data being transferred would require a modification of Estakhri et al., Iwata et al. and Harper, III et al. to disclose not only a copy-back command, but to allow for data transfer out of the Flash memory device and/or masking of the transferred data during a copy-back command, there would therefore be no motivation for one skilled in the art do so and the references do not disclose or suggest a motivation for doing so. In addition, Applicant further notes that, since neither Estakhri et al., Iwata et al. and Harper, III et al. disclose split data (storing user data in a differing word line or erase block from the associated overhead data) or operation or control circuits for managing the same, there would also be no motivation for one skilled in the art do so and the references do not disclose or suggest a motivation for doing so.

As detailed above, Applicant finds no motivation or suggestion to modify the operation of Estakhri et al., Iwata et al. and Harper, III et al. expressly or impliedly contained in the references, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the references. Applicant thus submits that the Office has also failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must

present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'"). Applicant therefore respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to the pending claims.

In regards to Gonzales et al. – Applicant respectfully maintains that Gonzales et al. discloses a non-volatile memory that operates to store variable data sizes and fields in each page of an erase block in order to more efficiently utilize the available memory storage. In this, Gonzales et al. discloses storing in a single page the associated overhead areas for user data areas store in two or more other pages or dividing a user data area and its associated overhead at a randomly selected point and storing them split across two pages. *See, e.g.*, Gonzales et al., Figures 2-9; Summary; Column 9, line 1 to Column 10, line 30. Applicant therefore maintains that Gonzales et al. does not disclose split data (storing user data in a differing word line or erase block from the associated overhead data) or a Flash memory with an internal copy-back or an internal modified copy back command or operation or control circuits for managing the same. Applicant therefore maintains that Gonzales et al. does not teach or suggest storing user data sectors or areas in two or more physical row pages, such that a first set of user data sectors are stored in a first physical row page along with the associated overhead data areas of a second set of user data sectors, and the associated overhead data areas of the first set of user data sectors are stored in a second physical row page along with the user data areas of the second set of user data sections (or a third set of user data sectors). Applicant also maintains that Gonzales et al. does not teach or suggest a split data non-volatile memory devices or systems as having split user/overhead data that avoids the issue of potential corruption of both the user data and overhead data due to each being held within close proximity to each other or on the same physical row (wordline), or super blocks as pairs of erase blocks where when user data is read from a sector of an erase block of the Flash memory, the overhead data for the user data is read from the overhead data area of a sector of the associated erase block of the erase block super block pair. *See*, Paragraphs [0010], [0025], [0035] and [0038] of the Specification of the Present Application. Applicant therefore maintains that Gonzales et al. does not teach or suggest the split data storage or a split or a non-split data move circuit or method of the claimed invention.

As such, Applicant submits that Gonzales et al. does not teach or suggest each and every element of the Applicant's claimed invention.

In regards to Miura et al. – Applicant respectfully maintains that Miura et al. discloses evaluating an ECC for data as it is transferred from a Flash memory to a DRAM device and not evaluating an ECC for user data as it is moved only within a Flash memory device itself or within a non-volatile memory system. *See, e.g.*, Miura et al., Paragraphs [0110]-[0114]. Applicant therefore maintains that Miura et al. does not disclose split data (storing user data in a differing word line or erase block from the associated overhead data) or a Flash memory with an internal copy-back or an internal modified copy back command or operation or control circuits for managing the same. Applicant also submits that Miura et al. does not teach or suggest evaluating an ECC for user data as it is moved within the Flash memory device or system or a split or a non-split data move circuit or method. As such, Applicant submits that Miura et al. does not teach or suggest each and every element of the Applicant's claimed invention.

Applicant thus submits that Estakhri et al., Iwata et al., and Harper, III et al. fail to teach or suggest such a split or a non-split data move circuit or method, either alone or in combination. Applicant also submits that Estakhri et al., Iwata et al., Harper, III et al., and Miura et al. fail to teach or suggest such a split or a non-split data move circuit and method, either alone or in combination.

Applicant submits Estakhri et al., Iwata et al., and Gonzales et al. fail to teach or suggest such a split or a non-split data move circuit or method, either alone or in combination. Applicant also submits Estakhri et al., Iwata et al., Gonzales et al., and Miura et al. fail to teach or suggest such a split or a non-split data move circuit or method, either alone or in combination.

As such, Applicant therefore submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. fail to teach or suggest all elements of Applicant's claimed invention.

Applicant's independent claims 1 and 85 recite, in part, a non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy-back move operation such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are

moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the at least one non-volatile memory device, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 1 and 85.

Applicant's independent claims 8, 16, 25, 36, 45, 54, 89, and 102 recite, in part, a split data move control circuit is adapted to move one or more selected user data sectors stored in two or more physical row pages of a selected source super block to a target super block such that the selected user data sectors stored in a first source physical row page of the source super block are moved to a first target physical row page of the target super block and the associated overhead data areas of the selected user data sectors stored in a second source physical row page of the source super block are moved to a second target physical row page of the target super block. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a split data move circuit adapted to move one or more selected user data sectors stored in two or more physical row pages of a selected source super block to a target super block, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 8, 16, 25, 36, 45, 54, 89, and 102.

Applicant's independent claims 29, 44, 46, and 101 recite, in part, a non-split data move control circuit, wherein the non-split data move control circuit is adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block of the one or more non-volatile memory devices such that the selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of a target erase

block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the one or more non-volatile memory devices, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a non-split data move circuit adapted to move one or more selected user data sectors and associated overhead data areas by reading the selected user data sectors and the associated overhead data areas into an internal latch of the one or more non-volatile memory devices, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 29, 44, 46, and 101.

Applicant's independent claims 69, 75, 84 and 93 recite, in part, reading data of a physical page row of a first source erase block of a source super block from a selected non-volatile memory device of one or more non-volatile memory devices; masking off a first selected range of data column bit values; writing the first selected range of data column bit values to a physical page row of a first target erase block of a target super block; reading data of a physical page row of a second source erase block of the source super block; masking off a second selected range of data column bit values; and writing the second selected range of data column bit values to a physical page row of a second target erase block of the target super block. Applicant submits Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., as detailed above, do not teach or suggest a method of moving data in super block, either alone or in combination. As such, Applicant submits that Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al. do not teach or suggest each and every element of claims 69, 75, 84 and 93.

Applicant respectfully contends that claims 1, 8, 16, 25, 29, 36, 44, 45, 69, 75, 84, 85, 89, 93, 101 and 102, as pending, have been shown to be patentably distinct from the cited references of Estakhri et al., Iwata et al., Harper, III et al., Gonzales et al., and Miura et al., either alone or in combination. As claims 2-7, 9, 11-15, 17, 19-21, 26-27, 30-33, 38-41, 67, 70, 73-74, 76, 78-79, 86-88, 90-92, 94-95 and 98 depend from and further define claims 1, 8, 16, 25, 29, 36, 45, 69, 75, 85, 89, and 93, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-9, 11-17, 19-21, 25-27, 29-33, 36, 38-41, 44-45, 67, 69-70, 73-76, 78-79, 84-95, 98 and 101-102.

Claims 63-64, 68 and 83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. (U.S. Published Application No. 2004/0193774) in view of Harper III, et al. (U.S. Patent No. 4,918,600). Applicant respectfully traverses these rejections and submits that claims 63-64, 68 and 83, as pending, are allowable for at least the following reasons.

Applicant respectfully maintains, as stated above, that Iwata et al. discloses a Flash memory card that has a Flash controller with an erase block data merge circuit which operates to consolidate data to a new erase block from an old erase block and subsequent erasure of the old erase block. Applicant maintains that, in disclosing a data merge circuit and operation, Iwata et al. does not disclose a modified copy back operation in a Flash memory or control circuits for managing the same. As noted by the Examiner, Iwata et al. also does not teach masking the read data. *See, e.g.*, Iwata et al., Figures 1, 4 and 5; Paragraphs [0016]-[0079] and [0111]-[0142]. In addition, as also stated above, Applicant respectfully maintains that Harper, III et al. discloses a memory system for dynamic address mapping for vector access and not a non-volatile memory system or masking a data move between erase blocks utilizing a modified copy back operation. Applicant also submits that Harper III, et al. does not disclose masking of data sectors read from the memory, but the masking of a row address field. *See, e.g.*, Harper, III et al., Figure 1; Column 14, lines 38-47; Abstract.

Applicant's independent claims 63 and 83 recite, in part, reading data of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices; transferring selected data from the selected non-volatile memory

device; masking off a first selected range of data column bit values; and writing the first selected range of data column bit values to a physical page row of a target erase block.

Applicant submits that Iwada et al. and Harper, III et al., as detailed above, do not teach or suggest a split or a non-split data move circuit or method utilizing a modified copy back operation in a non-volatile memory, either alone or in combination. As such, Applicant submits that Iwada et al. and Harper, III et al. do not teach or suggest each and every element of claims 63 and 83.

Applicant respectfully contends that claims 63 and 83, as pending, have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 64 and 68 depend from and further define claim 63, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 63-64, 68 and 83.

Allowable Subject Matter

Applicant acknowledges that claims 46-62 were indicated as being allowed in the Office Action.

Claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97, 99-100 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Applicant respectfully submits that it has been shown in this Office Action response that independent base claims 8, 16, 25, 29, 36, 63, 69, 75 and 93 have been shown to be patentably distinct from the cited references and are in condition for allowance. Claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97, 99-100 are also believed to be in condition for allowance in that these claims all depend from and further define their respective patentably distinct independent base claims. Applicant therefore respectfully requests reconsideration and withdrawal of the objections and allowance of claims 10, 18, 22-24, 28, 34-35, 37, 42-43, 65-67, 71-72, 77, 80-82, 96-97, 99-100.

CONCLUSION

Paragraphs [0038], [0045], [0046], [0064] and [0066] of the Specification have been amended. Figure 5A has been amended and a Figure 5A Replacement Sheet is attached. Claims 1-102 are pending.

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: 3/26/07

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